図 1

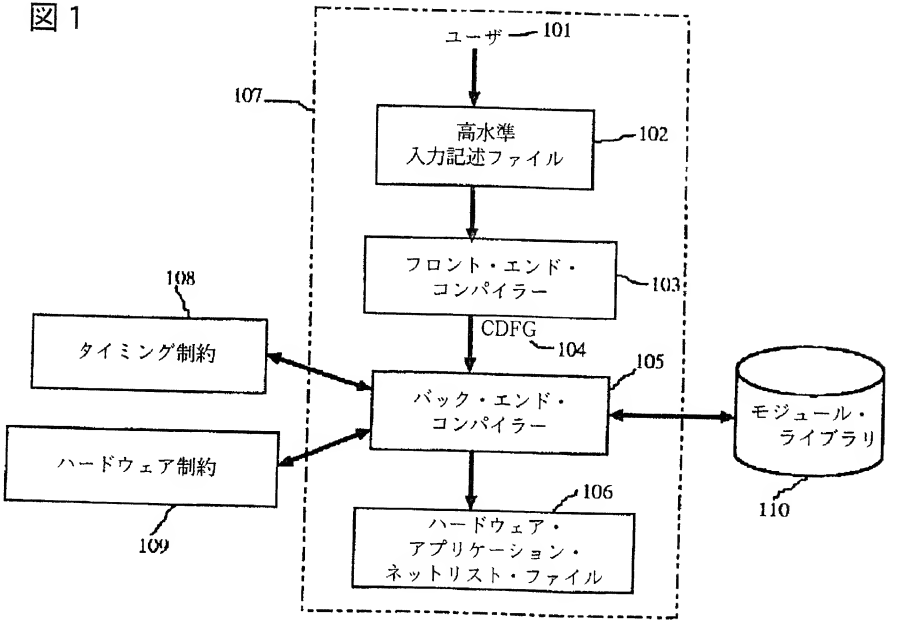


図２ａ

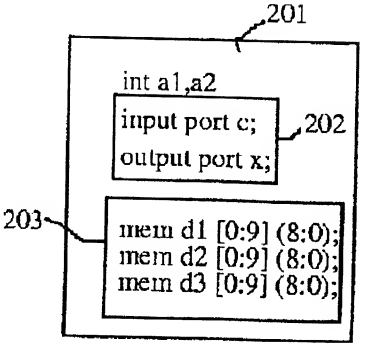


図２ｂ

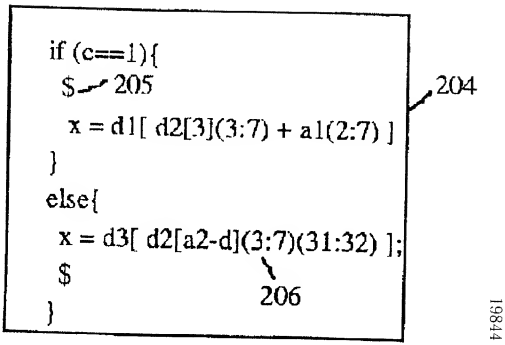
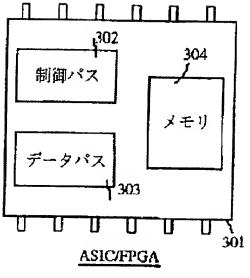
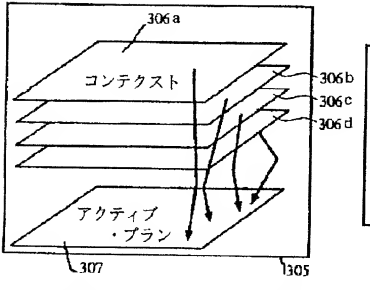


図 3


302
制御パス
304
メモリ
データパス
303
301
ASIC/FPGA


306 a
コンテクスト
306 b
306 c
306 d
アクティブ
・プラン
307
305
Dynamic Reconfigurable Hardware (DRL)

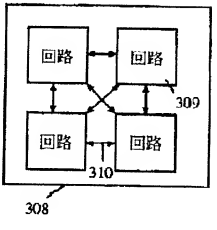

回路
回路
309
回路
回路
310
308
Multi-chip circuit

図 4

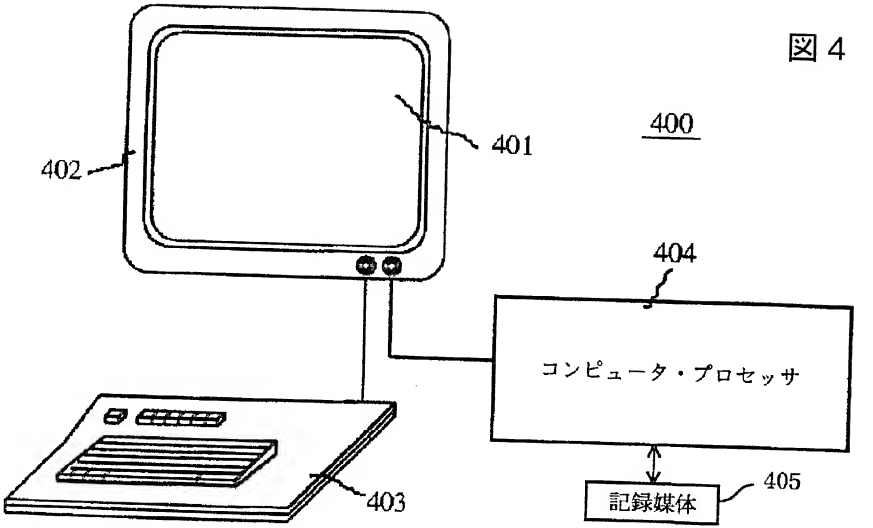


図 5

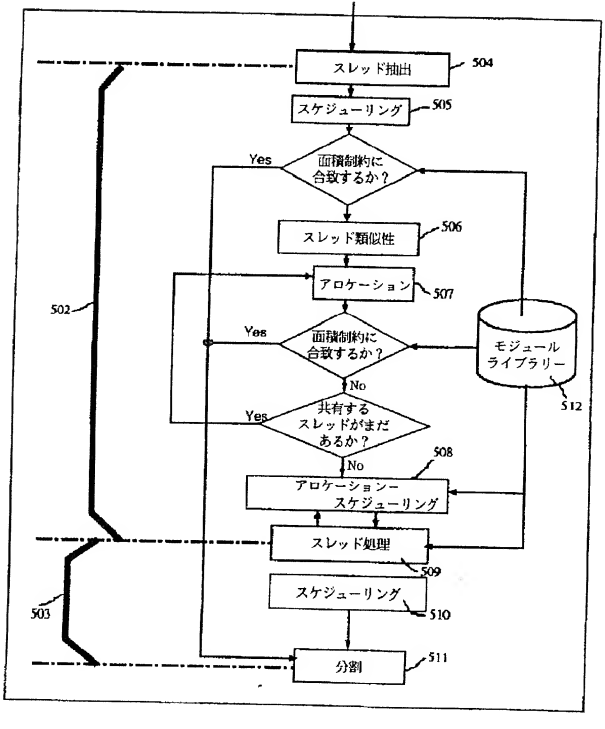

スレッド抽出
504
スケジューリング
505
Yes
面積制約に
合致するか？
スレッド類似性
506
アロケーション
507
502
Yes
面積制約に
合致するか？
モジュール
ライブラリー
512
No
Yes
共有する
スレッドがまだ
あるか？
No
508
アロケーション
スケジューリング
スレッド処理
509
スケジューリング
510
503
分割
511

図 6

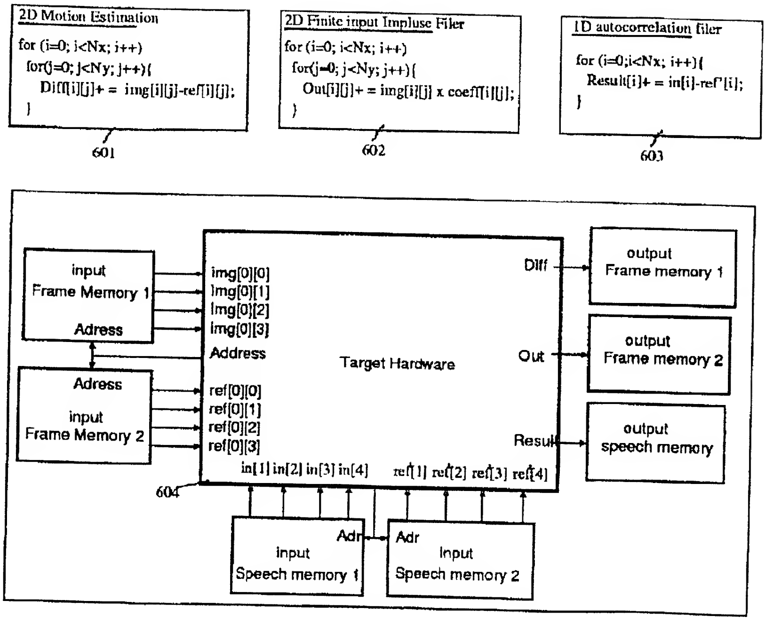
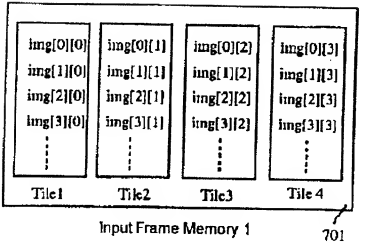
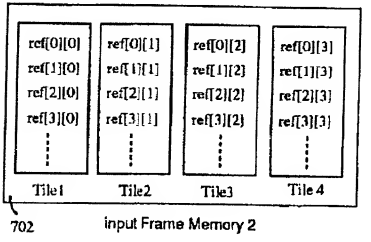

2D Motion Estimation
for (i=0; i<Nx; i++)
for(j=0; j<Ny; j++){
Diff[i][j]+ = img[i][j]-ref[i][j];
}
601
2D Finite input Impluse Filer
for (i=0; i<Nx; i++)
for(j=0; j<Ny; j++){
Out[i][j]+ = img[i][j] x coeff[i][j];
}
602
1D autocorrelation filer
for (i=0;i<Nx; i++){
Result[i]+ = in[i]-ref'[i];
}
603
input
Frame Memory 1
Adress
Adress
input
Frame Memory 2
img[0][0]
Img[0][1]
Img[0][2]
Img[0][3]
Address
ref[0][0]
ref[0][1]
ref[0][2]
ref[0][3]
Target Hardware
Diff
Out
Result
in[1] in[2] in[3] in[4]
ref[1] ref[2] ref[3] ref[4]
output
Frame memory 1
output
Frame memory 2
output
speech memory
604
Adr
input
Speech memory 1
Adr
Input
Speech memory 2

図 7


img[0][0]
img[1][0]
img[2][0]
img[3][0]
img[0][1]
img[1][1]
img[2][1]
img[3][1]
img[0][2]
img[1][2]
img[2][2]
img[3][2]
img[0][3]
img[1][3]
img[2][3]
img[3][3]
Tile1
Tile2
Tile3
Tile 4
Input Frame Memory 1
701


ref[0][0]
ref[1][0]
ref[2][0]
ref[3][0]
ref[0][1]
ref[1][1]
ref[2][1]
ref[3][1]
ref[0][2]
ref[1][2]
ref[2][2]
ref[3][2]
ref[0][3]
ref[1][3]
ref[2][3]
ref[3][3]
Tile1
Tile2
Tile3
Tile 4
702
input Frame Memory 2

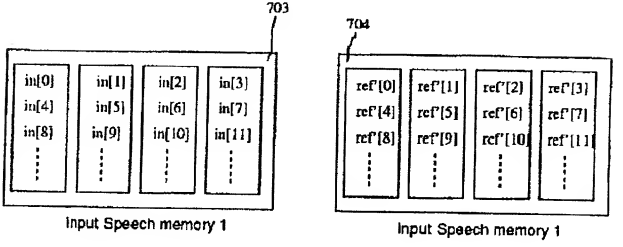

703
704
in[0]
in[4]
in[8]
in[1]
in[5]
in[9]
in[2]
in[6]
in[10]
in[3]
in[7]
in[11]
ref'[0]
ref'[4]
ref'[8]
ref'[1]
ref'[5]
ref'[9]
ref'[2]
ref'[6]
ref'[10]
ref'[3]
ref'[7]
ref'[11]
Input Speech memory 1
Input Speech memory 1

図 8

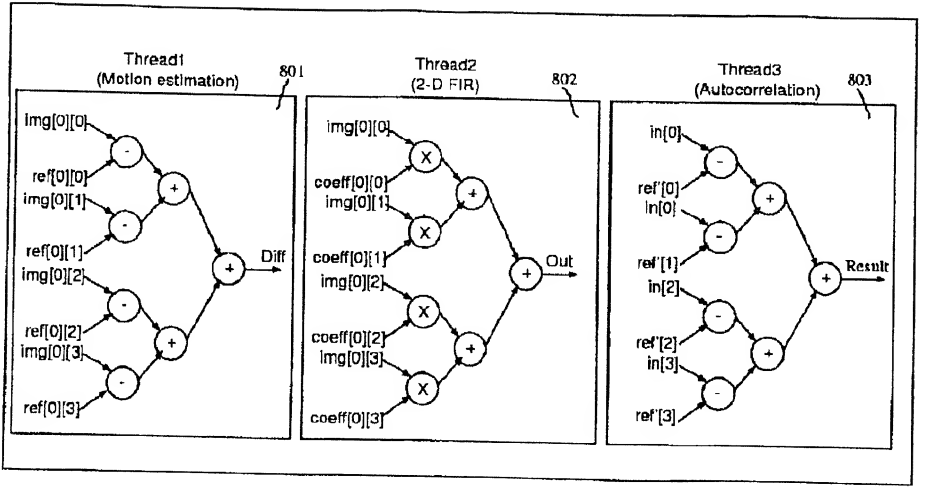


図 9

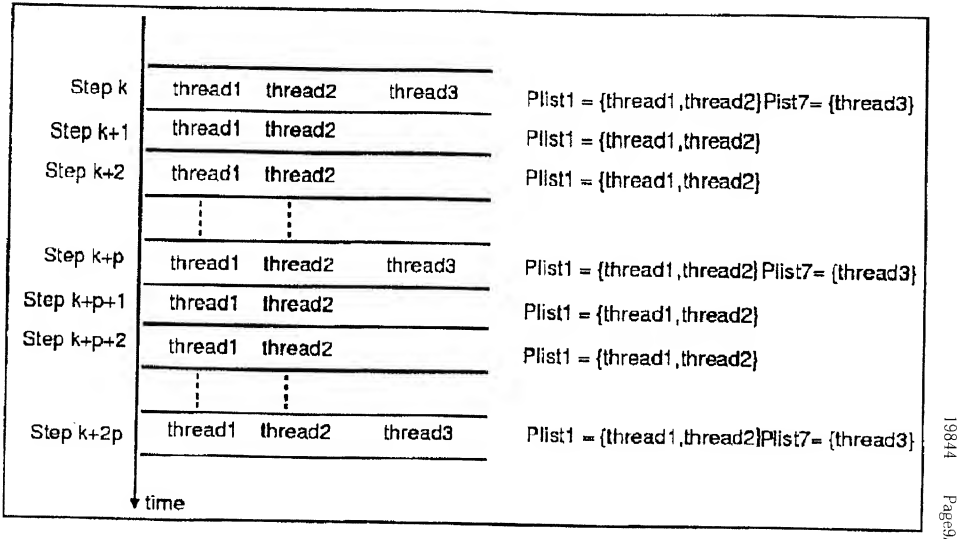
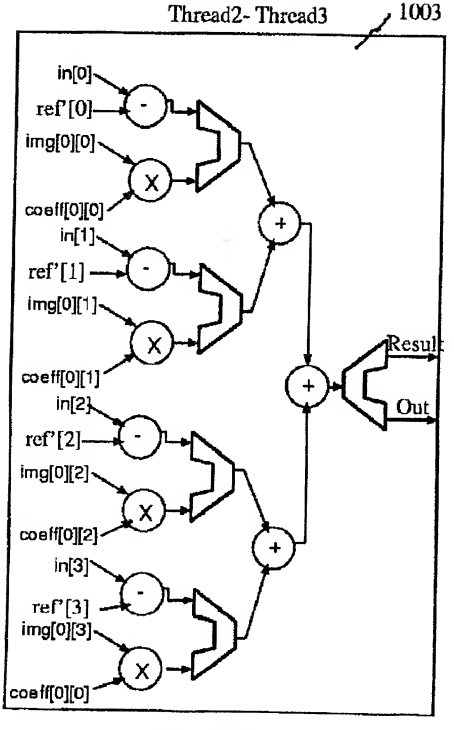


図１０



Area13 = 410

図11a

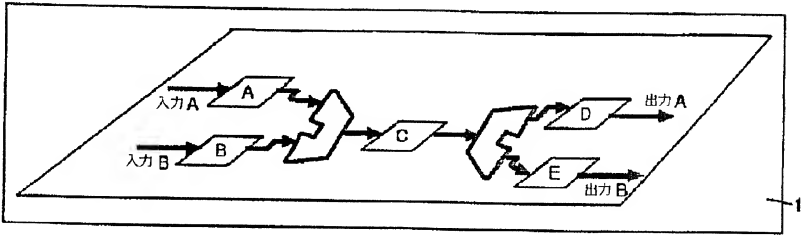
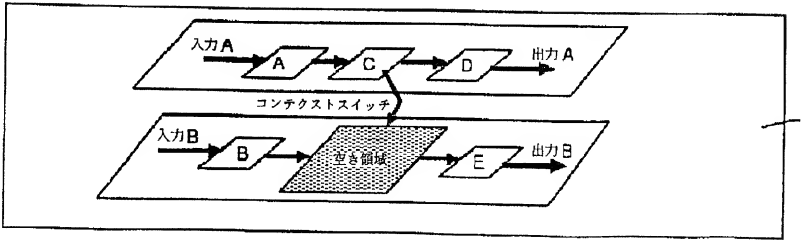


図11b



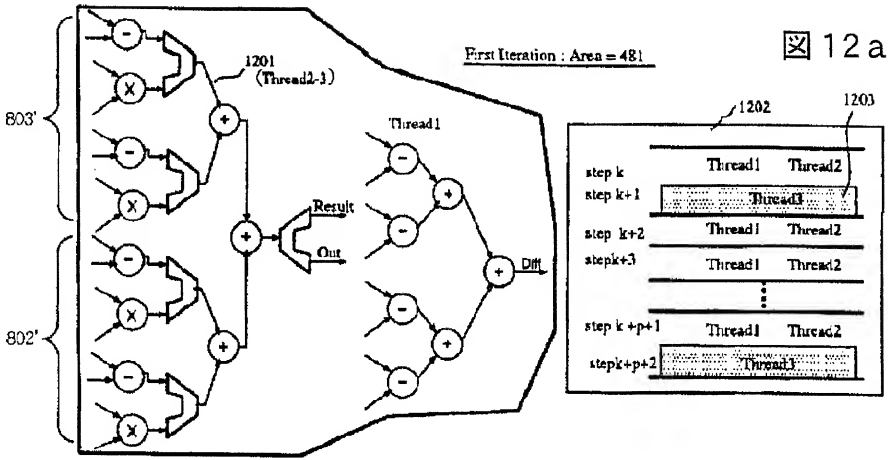
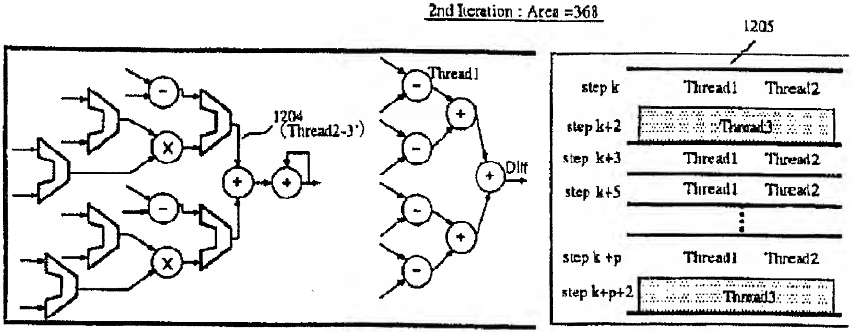


図 12 a

図 1 2 b


2nd Iteration : Area =368
1204
(Thread2-3')
Thread1
Diff
1205
step k
Thread1
Thread2
step k+2
Thread3
step k+3
Thread1
Thread2
step k+5
Thread1
Thread2
step k +p
Thread1
Thread2
step k+p+2
Thread3

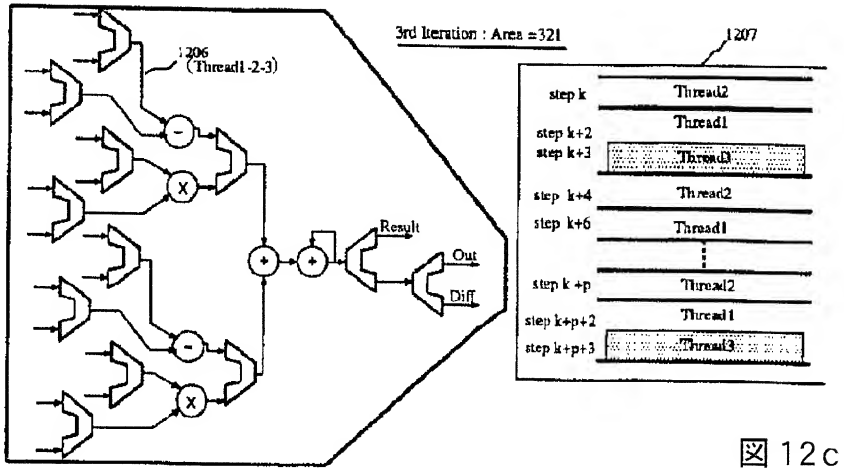
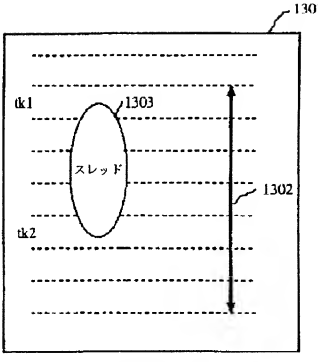
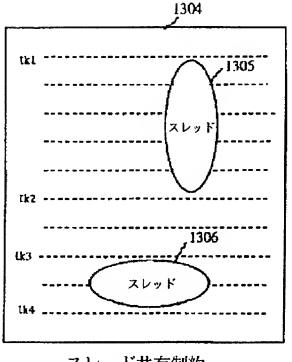


図 12c

図13a

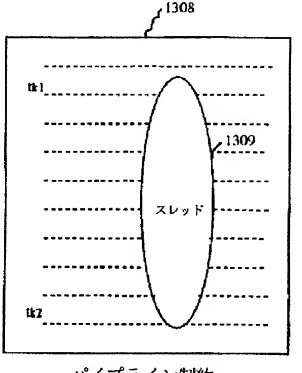


スレッド移動レンジ制約



スレッド共有制約

図13b



パイプライン制約

図13c

図14

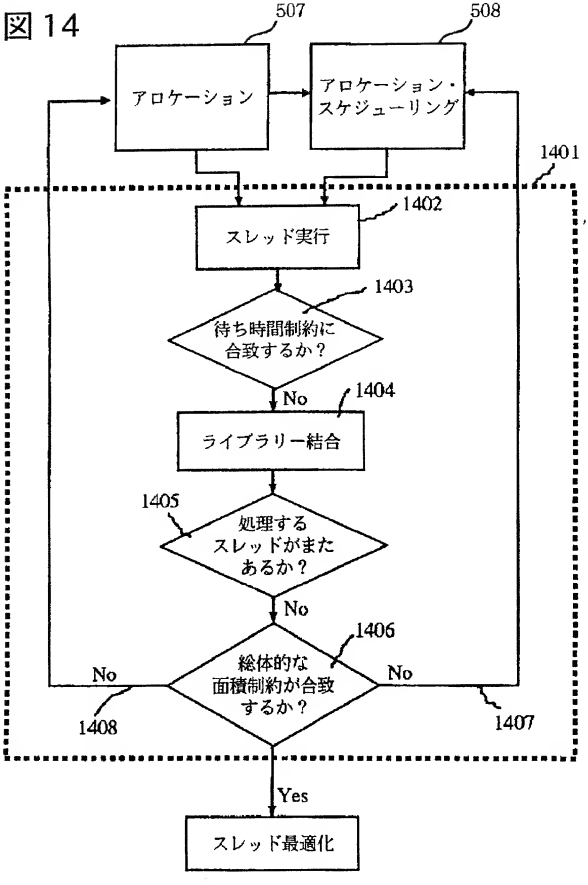

507
508
アロケーション
アロケーション・スケジューリング
1401
1402
スレッド実行
1403
待ち時間制約に合致するか？
No
1404
ライブラリー結合
1405
処理するスレッドがまたあるか？
No
1406
総体的な面積制約が合致するか？
No
No
1408
1407
Yes
スレッド最適化

図15

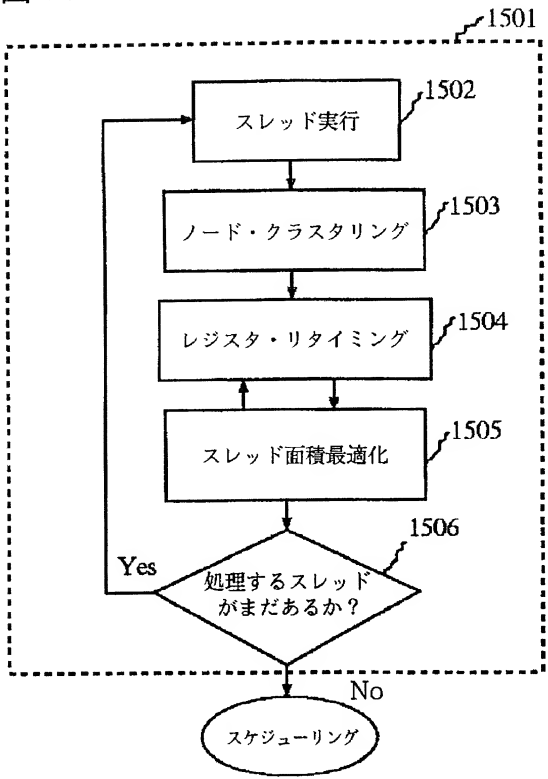

1501
スレッド実行
1502
ノード・クラスタリング
1503
レジスタ・リタイミング
1504
スレッド面積最適化
1505
処理するスレッドがまだあるか？
1506
Yes
No
スケジューリング

図16

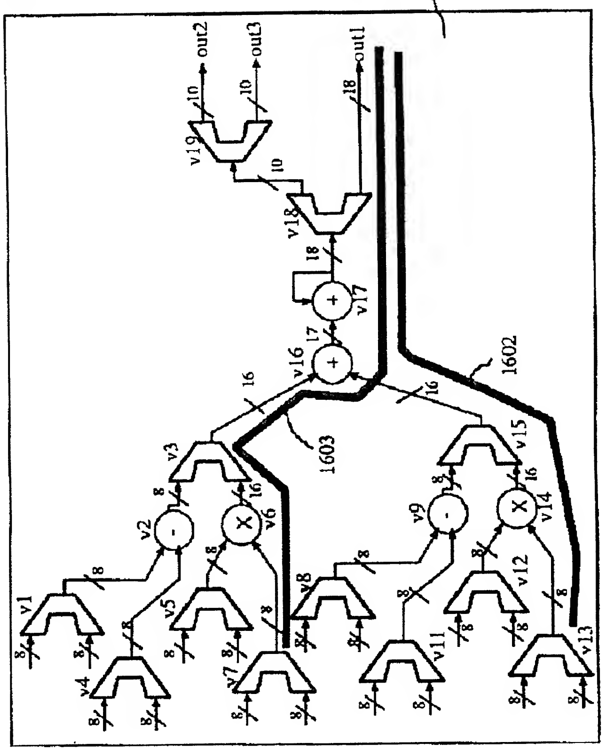

1601
1602
1603
out1
out2
out3
v1
v2
v3
v4
v5
v6
v7
v8
v9
v11
v12
v13
v14
v15
v16
v17
v18
v19

図 17

Closeness matrix

	v1	v2	v3	v4	v5	v6	v7	v8	v9	v10	v11	v12	v13	v14	v15	v16	v17	v18	v19
v1	—	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
v2	8	8	8	8	—		—	—	—	—	—	—	—	—	—	—	—	—	—
v3	—	8		—	—	16	—	—	—	—	—	—	—	—	—	16	—	—	—
v4	—	8		—	—		—	—	—	—	—	—	—	—	—	—	—	—	—
v5	—	—		—	—	8	—	—	—	—	—	—	—	—	—	—	—	—	—
v6	—	—	16	—	8		8	—	—	—	—	—	—	—	—	—	—	—	—
v7	—	—	—	—	—	8	—	—	—	—	—	—	—	—	—	—	—	—	—
v8	—	—	—	—	—	—	—	—	8	—	—	—	—	—	—	—	—	—	—
v9	—	—	—	—	—	—	—	8	—	—	8	—	—	—	8	—	—	—	—
v10	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
v11	—	—	—	—	—	—	—	—	8	—	—	—	—	—	—	—	—	—	—
v12	—	—	—	—	—	—	—	—	—	—	—	—	—	8	—	—	—	—	—
v13	—	—	—	—	—	—	—	—	—	—	—	—	—	8	—	—	—	—	—
v14	—	—	—	—	—	—	—	—	—	—	—	8	8	—	8	—	—	—	—
v15	—	—	—	—	—	—	—	—	8	—	—	—	—	8	—	16	—	—	—
v16	—	—	16	—	—	—	—	—	—	—	—	—	—	—	16	—	17	—	—
v17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	17	—	18	—
v18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	18	—	10
v19	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	10	—

1604

図18

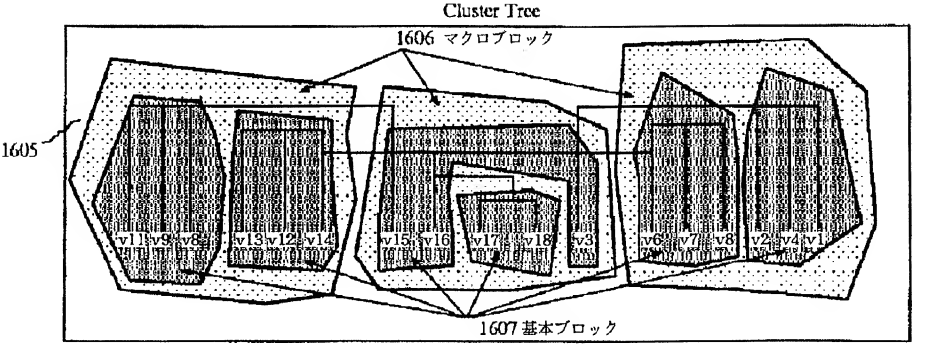
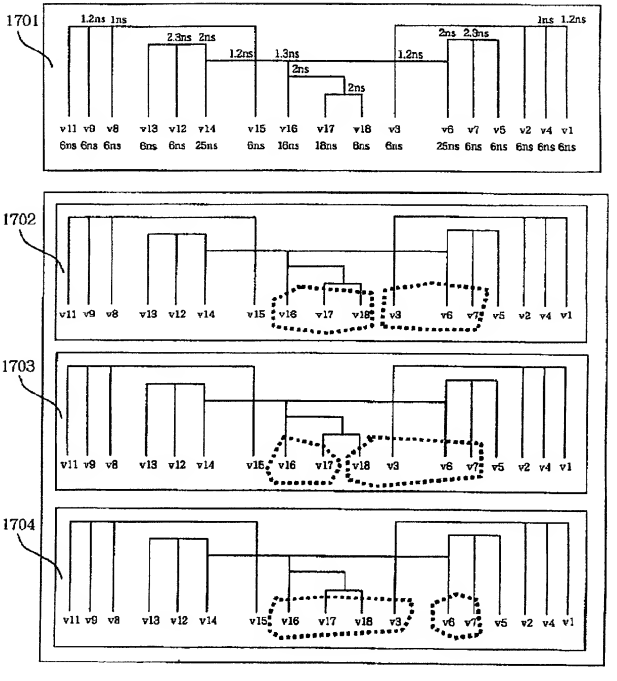

Cluster Tree
1606 マクロブロック
1605
v11 v9 v8
v13 v12 v14
v15 v16
v17 v18
v3
v6 v7 v8
v2 v4 v1
1607 基本ブロック

図19


1701
1.2ns 1ns
2.3ns 2ns
1.2ns
1.3ns
2ns
2ns
1.2ns
2ns 2.3ns
1ns 1.2ns
v11 v9 v8 v13 v12 v14 v15 v16 v17 v18 v3 v6 v7 v5 v2 v4 v1
6ns 6ns 6ns 6ns 6ns 25ns 6ns 16ns 16ns 6ns 6ns 25ns 6ns 6ns 6ns 6ns 6ns
1702
1703
1704